MegaPower Semiconductor

Si3981DV

Dual P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
–20	0.185 @ V_{GS} = –4.5 V	–1.9
	0.260 @ V_{GS} = –2.5 V	–1.6
	0.385 @ V_{GS} = –1.8 V	–0.7

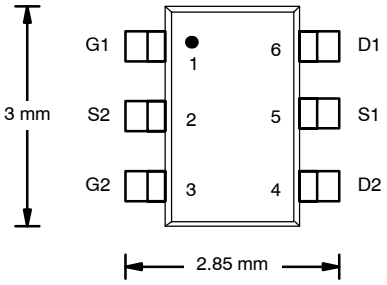
FEATURES

- TrenchFET® Power MOSFET

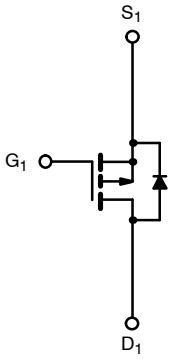
APPLICATIONS

- Battery Switch for Portable Devices
- Computers
  - Bus Switch
  - Load Switch

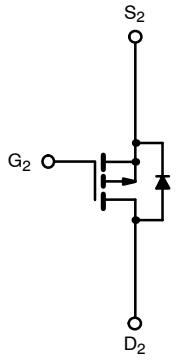
TSOP-6
Top View



Ordering Information: Si3981DV-T1—E3
Marking Code: MCxxx



P-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	5 secs	Steady State	Unit
Drain-Source Voltage		V_{DS}	–20		V
Gate-Source Voltage		V_{GS}	±8		
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	–1.9	–1.6	A
	T_A = 70°C		–1.5	–1.3	
Pulsed Drain Current		I_{DM}	–8		
Continuous Diode Current (Diode Conduction)[a]		I_S	–1.0	–0.72	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	1.08	0.80	W
	T_A = 70°C		0.69	0.51	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 5 sec	R_{thJA}	97	115	°C/W
	Steady State		132	155	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	78	95	

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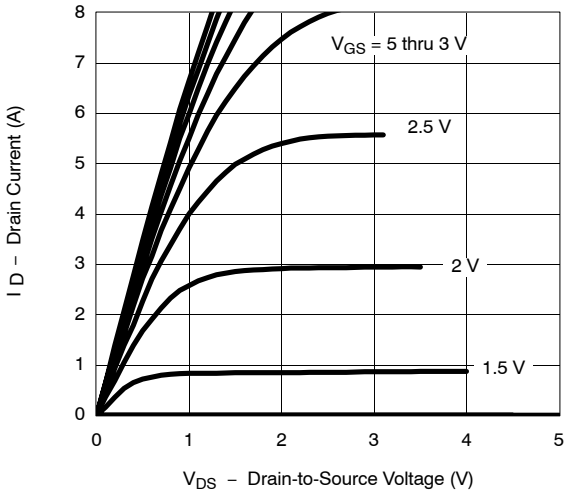
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −250 μA	−0.40		−1.1	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±8 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −20 V, V_{GS} = 0 V			−1	μA
		V_{DS} = −20 V, V_{GS} = 0 V, T_J = 85°C			−10	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = −5 V, V_{GS} = −4.5 V	−5			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = −4.5 V, I_D = −1.9 A		0.146	0.185	Ω
		V_{GS} = −2.5 V, I_D = −1.6 A		0.210	0.260	
		V_{GS} = −1.8 V, I_D = −0.7 A		0.306	0.385	
Forward Transconductance[a]	g_{fs}	V_{DS} = −5 V, I_D = −1.9 A		4		S
Diode Forward Voltage[a]	V_{SD}	I_S = −1.0 A, V_{GS} = 0 V		−0.84	−1.1	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = −10 V, V_{GS} = −4.5 V, I_D = −1.9 A		3.2	5	nC
Gate-Source Charge	Q_{gs}			0.42		
Gate-Drain Charge	Q_{gd}			0.84		
Gate Resistance	R_g	f = 1 MHz		6		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = −10 V, R_L = 10 Ω I_D ≅ −1 A, V_{GEN} = −4.5 V, R_g = 6 Ω		30	45	ns
Rise Time	t_r			50	85	
Turn-Off Delay Time	$t_{d(off)}$			45	85	
Fall Time	t_f			21	50	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = −1.00 A, di/dt = 100 A/μs		20	40	

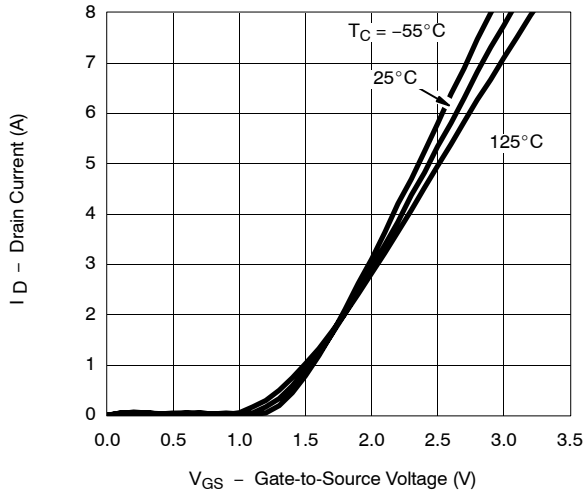
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

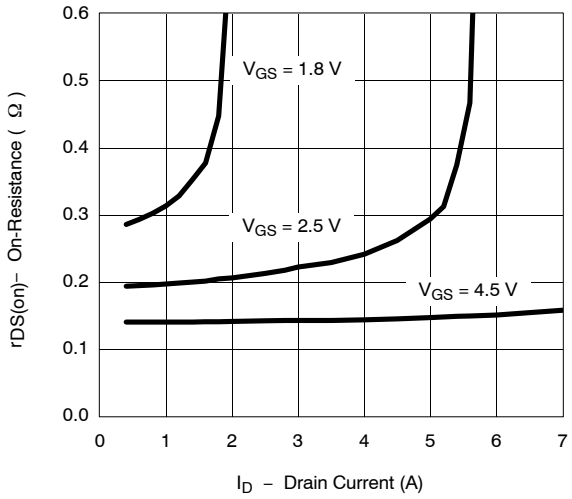
Output Characteristics



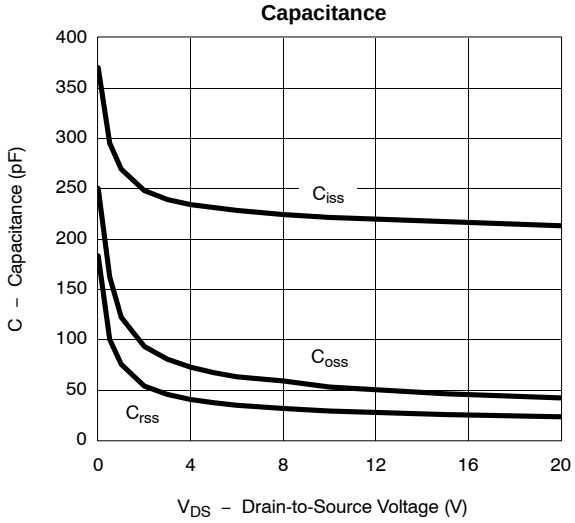
Transfer Characteristics



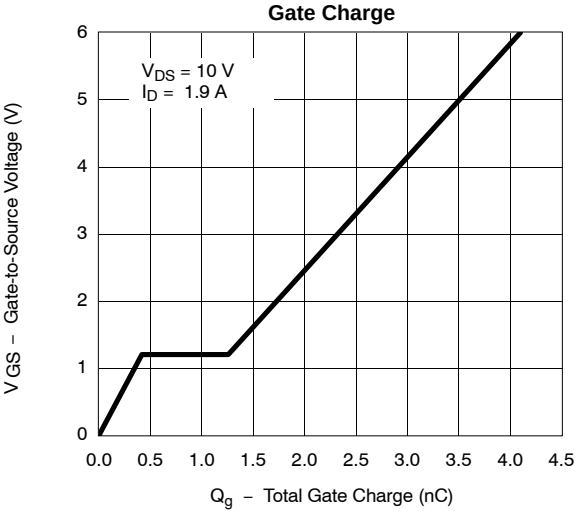
On-Resistance vs. Drain Current



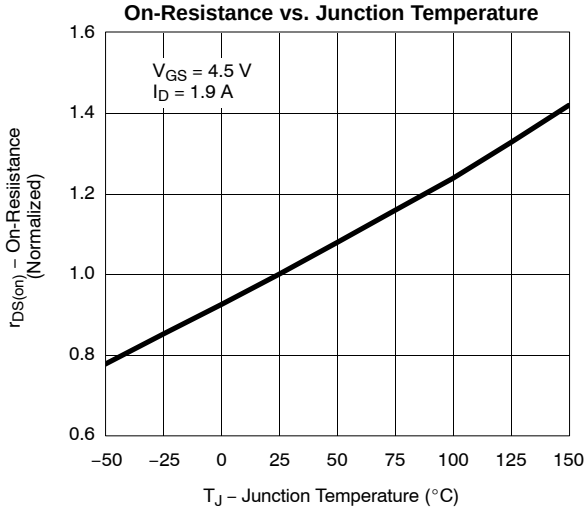
Capacitance



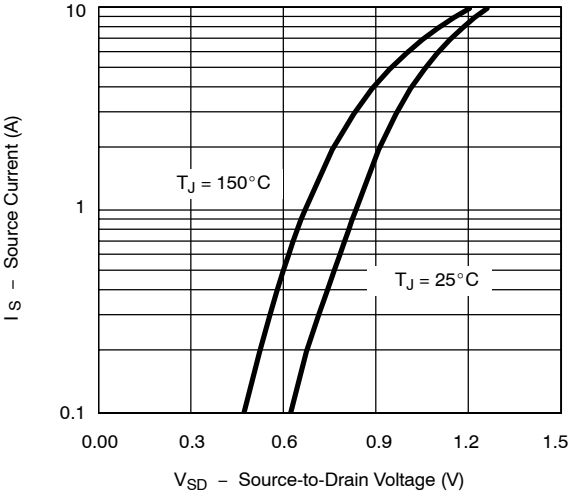
Gate Charge



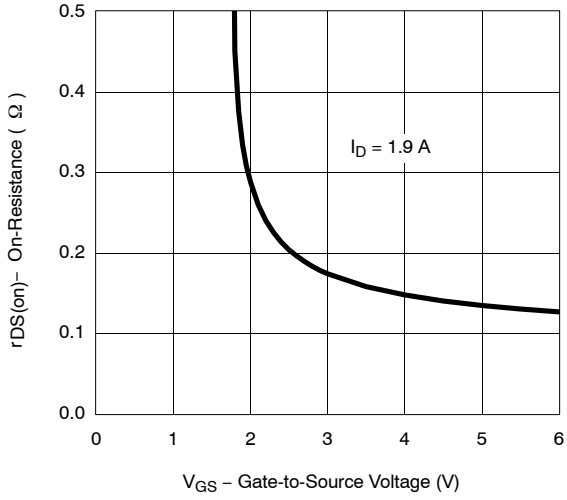
On-Resistance vs. Junction Temperature

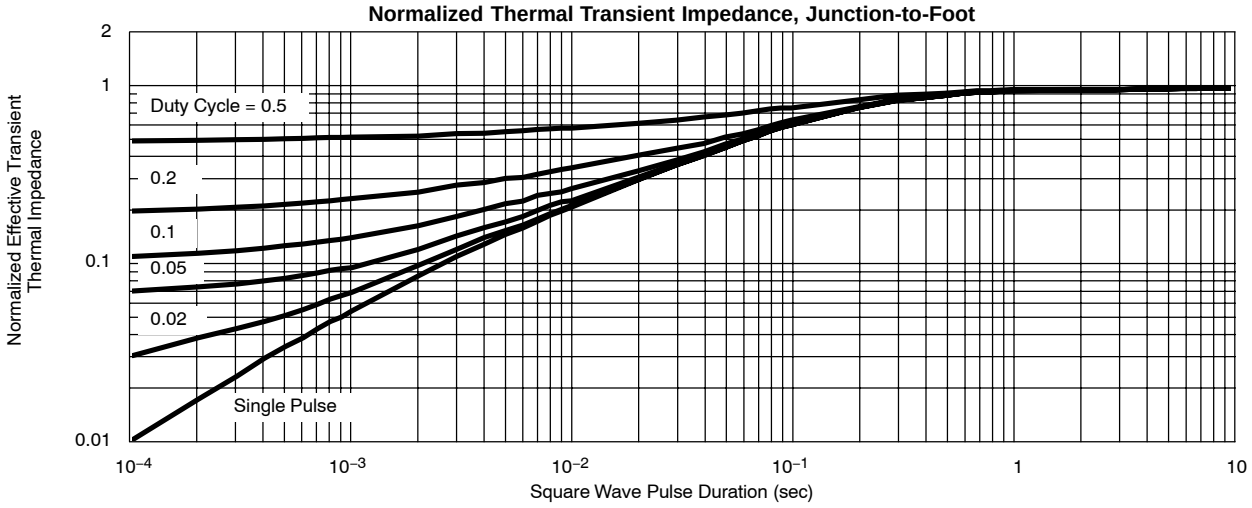


Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage




Normalized Thermal Transient Impedance, Junction-to-Foot
Normalized Effective Transient Thermal Impedance
2
1
0.1
0.01
Duty Cycle = 0.5
0.2
0.1
0.05
0.02
Single Pulse
10–4
10–3
10–2
10–1
1
10
Square Wave Pulse Duration (sec)